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ENTITLED

CUSTOM CLOCK INTERCONNECTS ON A  
STANDARDIZED SILICON PLATFORM

**CUSTOM CLOCK INTERCONNECTS  
ON A STANDARDIZED SILICON PLATFORM  
FIELD OF THE INVENTION**

The present invention relates to integrated circuits. In particular, the  
5 present invention relates to generation of clocks and resets in silicon  
platform chips.

**BACKGROUND OF THE INVENTION**

In design processes for very large scale integration (VLSI)  
10 integrated circuit chips, standard features and custom features can be  
combined to produce a completed design. The balance between use of  
standard and custom features is a difficult one that affects design costs,  
risks and time-to-market schedules and is often based on market forces  
that set performance requirements, unit costs, volume and design life for  
15 the finished integrated chip.

As illustrated in FIG. 1, different design process technologies lead  
to different mixes of time-to-market and performance. In FIG. 1, a  
vertical axis 100 represents relative performance in terms of speed and  
complexity of the functions performed by a chip. A horizontal axis 102  
20 represents relative time lengths of the design process for the chip.

A technology known as field programmable gate array (FPGA)  
typically produces designs indicated at 104 with ranges of relatively low  
performance, and medium time-to-market. With FPGA technology, an  
integrated circuit manufacturer places fixed gates in fixed patterns on  
25 chips and provides a fixed but "programmable" array of interconnects.  
The customer can then alter the interconnects on each chip, typically by  
damaging an interconnect with an overcurrent, to customize each gate

array chip for a particular application. Because the “building blocks” for this technology are system gates or other medium scale logic elements, the complexity that can be achieved is limited.

A technology known as application specific integrated circuitry (ASIC) typically produces designs indicated at 106 with ranges of relatively high performance and high time-to-market. With ASIC, an integrated circuit manufacturer provides a library of low to medium complexity cells such as logic gates, counters and latches. The integrated circuit manufacturer also provides or specifies software tools so that a customer can design, simulate and time the customer’s circuit. This logical representation is translated into a custom layout and custom interconnect of library and sometimes custom integrated circuits. Once the customer’s design is complete, then the integrated circuit manufacturer uses the customer’s design to manufacture custom chips with a custom interconnect pattern and also custom cell patterns. The design process is long because of the ever-increasing complexity associated with the open-ended nature of this process.

A design process known as application specific standard product (ASSP) typically produces designs indicated at 108 with ranges of relatively medium performance and low time-to-market. With ASSP, an integrated circuit manufacturer completes the design process for a chip (in much the same manner that a customer would complete a design process for an ASIC). Once the design is complete, then the integrated circuit manufacturer uses the design to make standard chips that are typically sold to multiple customers with similar needs, typically in a particular application niche. The use by multiple customers increases the volume and allows for a larger investment in the design process.

A more recent design process referred to here as a "standardized silicon platform" has a capability to produce designs indicated at 110 with ranges of performance and time-to-market that are comparable to FPGA, ASSP and ASIC, and also has a capability to produced designs in  
5 ranges outside of range of capabilities of FPGA, ASSP and ASIC. With standardized silicon platform technology, the manufacturer provides a partially manufactured very large scale integration (VLSI) standard integrated circuit that includes standard slices that are designed to perform complex, high level functions, but which have not had all of  
10 their associated interconnect layers completed. The integrated circuit manufacturer provides or specifies software design tools that enable a customer to integrate and customize these complex high level functions, thereby providing a very high level, fast design tool. The customer can also add in the customer's customized circuitry on the same chip. Once  
15 the customer's design is complete, the completed chip can be much more quickly produced since a significant portion of the problem is already solved. The time needed to integrate and customize the standardized silicon platform is small in comparison to ASIC technology. High relative levels of performance can be achieved with standardized silicon  
20 platform technology.

Within the entire design space, one area that can cause great difficulty across the spectrum of design activities is the generation, management, qualification and testing of clocking and reset circuitry. The standardized silicon platform technology includes the use of  
25 clocking and reset circuitry. Clock and reset circuitry is used to generate synchronized clock signals to meet the customer's specification for speed, sequencing, skew and other parameters. It is found however, that

in many cases the clock and reset circuitry is done in a way that is not compatible with the capabilities of the design systems available. There are many ways to create and manage these circuits poorly. As a result, they are often not able to meet complex clocking requirements that are  
5 unique to each customer's application. In addition, if these circuits are designed outside the capabilities of the design system, severe delays can be and are encountered in the overall development of the circuit. Implementation of complex "ad hoc" clock and reset circuitry is often difficult to test using EDA tools, slows down the circuit design process,  
10 and introduces considerable technical risk into the performance of the chip. The "ad hoc" circuitry is difficult to test using standard manufacturing test software tools, leaving potential open loop timing closure problems in the design.

A method and apparatus are needed that provide an increased  
15 level of standard clock and reset functionality and that reduce or eliminate the need for "ad hoc" customer circuitry for producing clocks that meet customer specifications.

#### SUMMARY OF THE INVENTION

20 Disclosed are a standardized silicon platform chip and methods for design of such chips. The standardized silicon platform chip comprises a substrate having a substrate surface that includes an array of unconnected transistors that surround a plurality of islands. The plurality of islands include circuit elements that are interconnectable  
25 within each island to form a plurality of varied circuit functions for each of the islands. The varied circuit functions include both application functions and clock functions.

The standardized silicon platform chip also comprises a plurality of interconnect layers deposited over the substrate surface. The interconnect layers interconnect the circuit elements within each island to complete the plurality of varied circuit functions.

5           The varied circuit functions include varied levels of integration including at least gates, flip-flops, clock trees, and oscillators. The varied circuit functions are custom connectable to the array of unconnected transistors to form standard clock resources for the standardized silicon platform chip.

10           In a preferred embodiment, a second plurality of interconnections the circuit elements on the islands and the array of unconnected transistors to form known good clock functions. The known good clock functions are selected from a group of clock functions that are known to provide superior performance in manufacturing test, timing closure,  
15           clocking functionality and other factors that impact time to complete a detailed design and manufacture of a standardized silicon platform integrated circuit.

            Other features and benefits that characterize embodiments of the present invention will be apparent upon reading the following detailed  
20           description and review of the associated drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a graph of relative performance as a function of time-to-market for different integrated circuit technologies.

25           FIGS. 2A illustrates a silicon wafer including an array of standardized silicon platform chips.

FIG. 2B illustrates an enlarged view of an exemplary chip in the array illustrated in FIG. 2A.

FIG. 2C illustrates an enlarged view of a small portion of the chip illustrated in FIG. 2B.

5        FIG. 3 illustrates a design tool and manufacturing process for producing a customized design for a standardized silicon platform chip.

FIG. 4 schematically illustrates clock resources for a standardized silicon platform chip.

10        DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the embodiments described below in FIGS. 2-4, a standardized silicon platform design technology is enhanced to include a method and apparatus for the creation of clocking and reset circuits with clock resources such as standard clock factories, standard oscillator sources  
15        and standard reset sources. Using a software design tool, the user can customize the clock resources to adapt them to the needs of a custom chip design specification. The use of complex, time consuming, risky add-ons of "ad hoc" circuitry is avoided. Once the custom design is quickly completed using the method and apparatus as expressed in a  
20        software design tool, this step of the chip is completed and ready to be passed on for design completion at the manufacturer.

FIG. 1 (discussed above in the background of the invention) defines the "standardized silicon platform technology" in a context of older technologies such as FPGA, ASIC and ASSP, which it can supplant.  
25        Standardized silicon platform technology includes the use of a silicon chip which has islands of circuit functions surrounded by an array of unconnected transistors that can be interconnected to form custom

application functions. As described below in connection with FIGS. 2A, 2B, 2C, 3, 4, the standardized silicon platform technology is extended to include standardized clock and reset designs that can be customized by addition of custom interconnect layers.

5           FIGS. 2A, 2B, 2C illustrate a standardized silicon substrate 132 that is enhanced to include standard clock resources on the substrate 132. Additional circuitry is added to the substrate 132 to effect customization of the clock resources in a context of the standardized silicon platform design process.

10           In FIG. 2A, a wafer 130 which uses standardized silicon platform technology is illustrated to include a large number of partially completed standardized silicon platform integrated circuits 132 arranged in a rectangular grid pattern on the wafer 130. In FIG. 2B, one of the partially completed standardized silicon platform integrated circuits 132 shown in  
15           FIG. 2A is enlarged to better show detailed features. The standardized silicon platform integrated circuit 132 includes slices 136, 142, 146 and clock resources including clock factories 138, 140, oscillator source 144 and reset source 148. The clock factories 138, 140 can be implemented using gate arrays or standard cells.

20           Each slice 136, 142, 146 comprises VLSI circuitry designed to perform a particular set of high level circuit functions. The pattern of slices and clock resources on each individual standardized silicon platform integrated circuit 132 is standardized for use in a particular marketing niche. Standardized silicon platform wafers 130 can be  
25           inventoried by the integrated circuit manufacturer for later use, if desired, to reduce time-to-market in customizing the standardized silicon platform wafer 130 in later processing steps which comprise



adding customized layers of interconnections. Each standardized silicon platform integrated circuit 132 is, however, only partially completed and does not include at least some interconnection layers that provide the customizing for a particular customer application. A standard design for the interconnection layers of each slice exists as a design stored in a computer, however, and is available to a customer as a design starting point for customizing.

A customer (user) may wish to customize the operation of a particular slice to meet a particular industry standard such as a communication protocol. A customer may also wish to customize a slice in order to provide a new product feature that differentiates the customer's product from competitor's products. A customer may also wish to customize a particular slice to meet other performance goals. Since the slice does not include all interconnection layers, the slice is not "hard wired" and interconnection patterns can be developed later and then applied to customize the slice. This customization can be done even though the standardized silicon platform wafer 130 is standardized.

Using the integrated circuit manufacturer's specified software design tools, the customer customizes the function of individual slices and also customized the design of interconnections between the slices. This customization is then implemented by generation of interconnection layer designs. At a later processing step, the standardized silicon platform wafer 130 will be diced to separate each integrated circuit 132 into an integrated circuit chip.

In FIG. 2C, a portion 134 of the standardized silicon platform integrated circuit 132 is illustrated to show exemplary details. In FIG. 2C, the substrate 132 has a substrate surface 150 that includes an array of

unconnected transistors 152 that surround islands 154, 156. The islands 154, 156 include circuit elements such as transistors 158, 160 that are interconnectable within each island to form a plurality of varied circuit functions for each of the islands 154. The varied circuit functions including both application functions and clock functions. As illustrated, islands 154, 156 form flip-flop functions.

A plurality of second interconnect layers 162, 164, 166, 168, 170 are deposited over the substrate surface 150. The second interconnect layers 162, 164, 166, 168, 170 interconnect the circuit elements (such as transistors 158, 160) within each island 154, 156 to complete the plurality of varied circuit functions. The varied circuit functions including varied levels of integration including at least gates, flip-flops, clock trees, and oscillators that are custom connectable to the array of unconnected transistors 152 to form standard clock resources for the standardized silicon platform integrated circuit 132. It will be understood by those skilled in the art that the interconnect layers are illustrated only schematically, and that actual interconnect layers are much more complex.

The particular application functions on the standardized silicon platform integrated circuit 132 are preferably selected to fill needs in a selected application niche. In a preferred arrangement, at least some of the varied circuit functions are connectable as both clock functions and application functions, depending on the needs for customization. The clock functions are preferably arranged to be connectable to form multiphase clock generators that generate a plurality of synchronous clock outputs with a closed timing specification. The array of unconnected transistors 152 preferably comprise N channel and P

channel field effect transistors as illustrated. When the custom interconnection layers are added, some of the unconnected transistors 152 are connected by the custom interconnections to perform circuit functions.

5           The pattern of interconnections that is designed by the customer customizes the function of one or more slices and also customizes the clock resources. The pattern of interconnections also customizes the interconnections between the slices, the clock resources and bonding pads (not illustrated). The design process for the customized  
10 interconnections 162, 164, 166, 168, 170 illustrated in FIG. 2C is described below in connection with FIG. 3. In a preferred arrangement, the customized interconnections are metallization layers. In particular, the process of including custom clock functions is described in FIG. 3.

FIG. 3 illustrates a software tool 200 and a manufacturing process  
15 224 for preparing standardized silicon platform integrated circuit chips that include customizable clock functions. The software tool 200 is preferably implemented as a computer readable medium having computer executable instructions for performing a custom integrated circuit design. The software tool is typically downloaded from a  
20 manufacturer's website to a user computer for execution by the user computer. As part of a standardized silicon platform design method, a standardized silicon platform wafer with standardized silicon platform integrated circuit substrates (such as wafer 130 of FIG. 2A) is formed. Each standardized silicon platform integrated circuit substrate (such as  
25 substrate 132 in FIG. 2B) comprises a plurality of standard slices (such as slices 136, 142, 146 in FIG. 2B) to form a standard slice substrate. Each integrated circuit substrate is also enhanced to include standard clock

resources. The standard clock resources comprise standard oscillator sources, standard reset sources, and standard clock factories.

A software design tool 200 illustrated in FIG. 3 is used to generate a custom clock distribution design as an integral part of a global interconnection design for all functions on the custom integrated circuit chip. As a starting point, a plurality of standard slice interconnection designs (not illustrated) corresponding with the plurality of standard slices are preferably available to the user in data form (as design starting points) but are not implemented in interconnections on the standardized silicon platform integrated circuit substrates 132. Because of the wide variety of clock requirements, however, a standard clock interconnection design is typically not available as a starting point for the user. Custom clock functions are included in a custom chip as part of a standardized silicon platform design method through the use of the software design tool 200.

The software design tool 200 generates a custom interconnection design (as physically realized in interconnection layers 162, 164, 166, 168, 170 in FIG. 2C) that includes a final custom clock distribution design 222 for application to the standard substrate in the manufacturing process 224 which applies custom interconnection to the standard substrate. The custom interconnection design defines interconnects that connect the custom clock resources (138, 140, 144, 148 in FIG. 2B). The custom interconnection design forms custom clock functions and defines interconnects that connect the custom clock functions to the standard slices (136, 142, 146 in FIG. 2B).

In the manufacturing process 224, a plurality of interconnection layers (such as layers 162, 164, 166, 168, 170) are applied to the standard

substrate (132 in FIG. 2A) according to the custom interconnection design to complete the custom chip with custom clock functions.

The software design tool 200 includes a resource selector 226. The resource selector 226 receives data resources 228 defining the standard  
5 substrate (134 in FIG. 2A) and user requirement for the custom chip. The resource selector 226 generates a design of the custom clock functions 230. The resource selector 226 examines the available resources and the customer requirements 232 and selects which device resources to use to compose a particular customer clock and reset requirement. The resource  
10 selector 226 passes this information to a composer 240 to generate the various clock and reset objects needed. The design 230 defines a circuit assembled from available clock resources at a boolean level. The design 230 does not necessarily completely define precisely which particular gate, counter or other clock resource is used and does not completely  
15 define interconnection patterns.

The data resources 228 preferably comprise clock and reset requirements data 232 specified by the user, data on standard clock resources 234, including known good clock circuits) available on the standard substrate and associated with the development process, data on  
20 electrical current resources 236 available, and physical layout data 238 for the standard substrate. The clock and reset requirements data 232 can include clock and reset domains, clock characteristics (skew targets, margin, cycle time, insertion latency), insertion latency targets, power management requirements, cross clock domain coupling, MFG test  
25 source oscillators, LBIST groupings.

The clock and reset composer 240 is provided as part of the software design tool 200. The clock and reset composer 240 generates a

custom clock distribution design 222 that defines the interconnects for the custom clock design. It will be understood that such definition of interconnects is preferably integrated into a definition of interconnects for the entire custom chip. The clock and reset composer 240 provides  
5 gross clock and reset design checking, comparisons between customer requirements and composed clock and reset performance. The clock and reset composer also provides calculations of insertion delays from physical placement information, clock skew estimations based on physical placement information, and requirements vs. selected options  
10 sanity checking. Other features include oscillator management, logical and physical clock and reset construction, clock and reset distribution control, fast clock and reset tuning, cross-domain clock tuning capability and integrated manufacturing tests.

The software design tool 200 generates iterative custom clock  
15 function designs 230 and iterative custom clock distribution designs 222 in which a present design iteration is a function of a previous design iteration. A previous design iteration is fed back along path 242 to the resource selector 226 in order that it can be used in a next design iteration.

20 A wrapper generator 244, a clock and reset compiler 246 and an ad hoc clock detector 245 preferably support the operation of the clock and reset composer 240. The ad hoc clock detector 245 provides a warning if the user has inadvertently included ad hoc clock circuitry in the design. If ad hoc clock circuitry is detected, it can be removed in a  
25 user interaction design closure function 247. The wrapper generator 244, based on the type of clock and reset pair being generated, creates the RTL and other structures required to provide the insertable clock and

reset objects as requested by the clock and reset composer 240. The clock and reset composer 240 generates resource vs requirements mismatch data 247 and views 248 (RTL view, synthesis view, STA view, test view) of the custom clock distribution design 222. The custom clock  
5 distribution design 222 is preferably tested by design qualifier 250 as part of a process of determining whether additional design iterations are needed to converge on a final version of design 222.

The design tool 200 provides the ability to compose clocks and resets from a combination of diffused and gate array clocking resources.  
10 The design tool 200 preferably has the ability to correct by construction test insertion and the ability to quickly and easily balance across multiple clock domains without user intervention. Use of the design tool 200 allows for intelligent composing of clocks and resets which leads to higher density of functionality on the substrate. The design tool 200  
15 provides performance feedback to the designer of the custom interconnection through the views 248, which reduces costly redesign late in the design cycle. The design tool preferably provides clock and reset structures that are known to be able to be processed through a bounded set of limits in the design system.

20 FIG. 4 schematically illustrates clock resources for a standardized silicon platform chip. In FIG. 4, the clock resources include standard oscillators 300, 302, 304, standard clock factories 306, 308, 310 and standard reset sources 312, 314, 316, 318. As illustrated in FIG. 4 the various resources are formed on the substrate missing the logical  
25 interconnections needed to make the various resources function. The various resources form a kit of standard components from which a complex clock circuit can be designed simply by design of a custom

interconnection pattern. These interconnections are provided in a later manufacturing step in the form of a custom pattern of interconnections.

Each of the standard oscillators 300, 302, 304 has input nodes that can be connected by the interconnections to either VDD or VSS to set a custom frequency. Each of the standard oscillators provides an oscillator output and has an oscillator reset input. The standard oscillator sources illustrated are examples, and other types of oscillators, such as phase lock loop oscillators can also be used as standard oscillator sources. Much larger numbers of standard oscillator sources can be used. The standard oscillator sources can include feature such as reference clock I/O, PLL's , gate arrays, DLLs and pre-partially integrated IP.

Each of the standard clock factories 306, 308, 310 includes a counter that has a clock input, a reset input, an up/down input and outputs Q0-Q7. Each clock factory 306, 308, 310 also has clocking constraints and decoding of the counter output. Much larger numbers of clock factories can be used. Fully formed clock and reset factory outputs can be distributed their destinations on the slices with the interconnections.

Each of the standard reset resources 312, 314, 316, 318 includes a large array of combinatorial logic (gates, flip flops, multiplexers, etc.) that can be connected to define complex reset conditions for resets to the standard oscillators and standard clock factories. Standard reset resources can include Reset I/O, reset registers and reset counters.

In a preferred embodiment, known good clock circuits are interconnected from the circuit elements on the islands and the array of unconnected transistors. The known good clock circuits are selected from a group of clock functions that are known to facilitate



manufacturing test, timing closure, clocking functionality and other factors that impact time to complete a detailed design and manufacture of a standardized silicon platform integrated circuit.

Standardized silicon platform design technology is enhanced to  
5 include a standard integrated circuit substrate with clock resources such as standard clock factories, standard oscillator sources and standard reset sources. Using a software design tool, the user can define interconnection patterns that customize the clock resources to adapt them to the needs of a custom chip design. The use of complex, time  
10 consuming, risky add-ons of "ad hoc" circuitry is avoided.

The software design tool is able to compose clocks and resets from a combination of diffused and gate array clocking resources. The software design tool is able to make corrections by construction test inserts, and is able to quickly balance across multiple clock domains. A  
15 highly flexible yet physically realizable set of clock and reset combinations is made available to the user. Clocks and resets are efficiently composed to conserve silicon real estate. An early view of the achievable clocking constructs and performance based on actual physical information is made available.

20 Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the scope of the invention.